

In re Patent Application of:
RAYNOR ET AL.
Serial No. 10/677,850
Confirmation No. 5132
Filed: **October 2, 2003**

REMARKS

Applicants would like to thank the Examiner for the thorough examination of the present application.

Applicants would also like to thank the Examiner for the courtesies extended during the telephone interview on April 24, 2008. During the interview, certain features of the claimed invention were discussed, including the recited "integrated circuit die" and "flip-chip arrangement" as understood in the art. During the interview, the Examiner asked that the Applicants provide a reference defining flip-chip technology so that he may rely on this in addition to what is disclosed in the specification. Each of the attached references are briefly discussed below:

1) Reference A is from the on-line Wikipedia encyclopedia, and is directed to a "flip chip." As stated in the first paragraph, a flip chip is one type of mounting used for semiconductor devices (such as IC chips), which is using solder bumps instead of wire bonds. The solder bumps are deposited on the chip pads, located on the top side of the wafer. To mount the chip to external circuitry on a circuit board, it is flipped around, i.e., the top side is facing down towards the mounting area. The solder bumps are used to connect directly to the associated external circuitry.

2) Reference B is also from the on-line Wikipedia encyclopedia, and is directed to a "flip chip." As stated in the first paragraph, a flip chip is one type of mounting used for semiconductor devices (such as IC chips), which does not require

In re Patent Application of:

RAYNOR ET AL.

Serial No. 10/677,850

Confirmation No. 5132

Filed: October 2, 2003

any wire bonds.

3) Reference C is from an on-line computer hardware and micro-scope glossary. On page 3/3, "chip" is defined as "a slang term for an integrated circuit."

4) Reference D is also from the on-line Wikipedia encyclopedia, and is directed to a "die." A die in the context of integrated circuits is a small block of semiconducting material, on which a given functional circuit is fabricated. Integrated circuits are typically produced in large batches on a single wafer. The wafer is then cut into many pieces, each containing one copy of the circuit. Each of these pieces is called a die.

The arguments supporting patentability of the claims are provided below.

I. The Claimed Invention

The present invention, as recited in independent Claim 39, for example, is directed to method of attaching a sensor and a housing to opposite sides of a mounting substrate. The sensor comprises an integrated circuit die having a sensing face and comprises a sensing area and at least one signal output contact thereon. The mounting substrate has a circuitry face and at least one signal input contact thereon. The mounting substrate also has an opening therethrough and at least one landing adjacent the opening. The method comprising positioning the sensing area over the opening so that the at least one signal output contact of the sensor contacts the at least one signal input contact of the

In re Patent Application of:
RAYNOR ET AL.
Serial No. **10/677,850**
Confirmation No. **5132**
Filed: **October 2, 2003**

mounting substrate.

The sensor is attached to the mounting substrate in a flip-chip arrangement with at least one bump bond interposed between the at least one signal output contact of the sensor and the at least one signal input contact of the mounting substrate to pass signals therethrough, with the at least one bump bond being associated with the at least one landing so that the at least one bump bond is aligned with the at least one signal output contact of the sensor. The housing is positioned in contact with the mounting substrate so that the housing and the sensor are in alignment.

Independent Claim 57 is directed to a method of attaching a sensor to a mounting substrate, and is similar to independent Claim 39.

II. The Claims Are Supported By The Specification

The Examiner rejected the claims as including subject matter not supported by the specification. In particular, independent Claims 39 and 57 each recite that the sensor comprises "an integrated circuit die." The Examiner has taken the position that an integrated circuit die is not supported by the specification.

The specification makes reference to "chip" in paragraphs 11-13, for example. As provided on page 3/3 in Reference C, "chip" is defined as "a slang term for an integrated circuit." In Reference D, a die is defined in the context of integrated circuits. A die is a small block of semiconducting

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

material, on which a given functional circuit is fabricated. Integrated circuits are typically produced in large batches on a single wafer. The wafer is then cut into many pieces, each containing one copy of the circuit. Each of these pieces is called a die.

Independent Claims 39 and 57 each recite that the sensor comprises "an integrated circuit die." The Applicants submit that one skilled in the art readily understands that to have an integrated circuit, you have to have a die. A die is at the heart of an integrated circuit. The Applicants thus submit that in view of the attached references C and D, the specification supports recitation of "integrated circuit die" in the claimed invention.

III. The Claims Are Patentable

The Examiner rejected independent Claims 39 and 57 over the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent.

The Venkat et al. patent discloses an integrated lens and aperture plate for an optical sensor equipped integrated chip in which the lens and the aperture plate are molded as one piece with the lens at the appropriate location so that the lens aligns with the location of the optical sensor. In particular, FIG. 2 in the Venkat et al. patent illustrates a sensor **32** being attached to a mounting substrate **36**. The sensor **32** is attached via the pins extending therefrom by inserting the pins through the openings in the mounting substrate **36**.

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

As correctly noted by the Examiner, Venkat et al. fails to disclose the use of bump bonding for attaching the sensor to the mounting substrate. The Examiner cited the Bauer et al. patent, and in particular FIG. 8 therein, as disclosing the use of bump bonding using solder bump **120** in attaching an optical sensor **22** to a mounting base substrate **28** that comprises circuitry (e.g., conductive strip **30**).

In addition, the Examiner cited Casson et al. as disclosing the attachment of a chip device to a flexible printed circuit board using solder bumps to facilitate a secure electrical connection. The Examiner referenced column 16, lines 52-68 as disclosing self-alignment of the chip device to the mounting substrate comprising a flexible printed circuit board using a solder bump bonding methodology that also comprises a heating step.

The Examiner has taken the position that a combination of known elements as disclosed by the cited prior art references would have been obvious to try. The Examiner further states that since the use of bump bonding in the assembly of integrated circuit and printed circuit board devices are well known, then it would have been obvious to a person of ordinary skill in the art to use bump bonding to facilitate an effective and secure alignment of the components of the claimed invention.

The Applicants respectfully disagree, particularly since Venkat et al. simply fails to teach or suggest that the sensor **32** may be mounted in a flip-chip arrangement. Instead, the sensor **32** is a packaged chip or die with a plurality of pins

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

extending therefrom. In addition, Venkat et al. does not make any reference to bump bonding since the sensor **32** is not in a flip-chip arrangement.

Definitions of a "flip chip" is provided in the attached References A and B. As stated in the first paragraph of Reference A, a flip chip is one type of mounting used for semiconductor devices (such as IC chips), which is using solder bumps instead of wire bonds. The solder bumps are deposited on the chip pads, located on the top side of the wafer. To mount the chip to external circuitry on a circuit board, it is flipped around, i.e., the top side is facing down towards the mounting area. The solder bumps are used to connect directly to the associated external circuitry. Reference B defines a flip chip as one type of mounting used for semiconductor devices (such as IC chips), which does not require any wire bonds. Consequently, Venkat et al. simply fails to teach or suggest that the sensor **32** may be mounted in a flip-chip arrangement.

While bump bonding is more commonplace today, the bump bonds in Bauer et al. are attached to a long conductive strip **30** which extends from near the aperture **122** outwards to the edge of the base substrate **28**, as shown in FIG. 8. The same conductive strip is used in all embodiments. It is also clear from FIG. 1 in Bauer et al. that the conductive strip is relatively wide. Bauer et al. is thus silent regarding the issue of alignment. In many of the embodiments, conventional wire contacts **32** are used in Bauer et al. for aligning the optical sensor **22** with the substrate **28**.

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

In Casson et al., the illustrated flip chip **10** fails to disclose a mounting substrate having an opening therethrough as in the claimed invention. Reference is directed to column 7, lines 7-21 of Casson et al., which provides:

"Referring to FIGS. 1a and 1b, a flip chip is an unpackaged silicon integrated circuit chip, such as flip chip **10**, having a silicon chip **17** containing the integrated circuit components and coated with an active side passivation layer **11a** on the active side **12** to protect its components from environmental contaminants. It has markings **13** applied to its back side **14** for identification purposes, and a back side passivation layer **11b** coated on back side **14** to protect the markings. It also has a number of aluminum/copper bonding pads, such as bonding pad **15**, which are located at various positions on the flip chip's active side for making electrical connections with a substrate. Solder bumps, such as solder bump **16**, are further attached to these bonding pads." (Emphasis added).

As best illustrated in FIGS. 1a and 1b and as stated above, Casson et al. teaches away from an opening in a mounting substrate associated with the flip chip **10** because of reflow of the soldering between the bonding pads **15** and the solder bumps **16** for providing the electrical connection.

As correctly noted by the Examiner in column 16, lines 52-68 of Casson et al., a solder composition is formed by reflowing solder paste located on the corresponding active contact pad on the circuit board such that a solder bump located

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

on the corresponding bonding pad on the flip chip is allowed to self-align with the corresponding active contact pad and such that the solder paste mixes with the solder bump, and wherein each electrical connection is formed concurrently by applying heat to the circuit board and flip chips as a whole after the flip chips have been placed on the circuit board in a manner which allows for unobstructed motion of the flip chips during reflow.

If there was an opening in the mounting substrate associated with the flip chip **10** in Casson et al. as in the claimed invention, then the soldering between the bonding pads **15** and solder bumps **17** would not be able to reflow as necessary for providing the desired electrical connection. As noted above, each electrical connection in Casson et al. is formed concurrently by applying heat to the circuit board and to the flip chips **10** as a whole after the flip chips have been placed on the circuit board in a manner which allows for unobstructed motion of the flip chips during reflow.

The Applicants submit that one skilled in the art would infer upon reading Venkat et al. that the wire bonds, together with their corresponding apertures, would not be necessary for ensuring an accurate alignment of the IC with the PCB. Venkat et al. is concerned with alignment of an integrated circuit sensor and the lens, and the approach taught is to integrate the lens with an aperture plate that also receives the IC **32**. In Venkat et al., conventional wire contacts are used for aligning the optical sensor IC **32** with the substrate. The whole

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

sensor/aperture plate/lens is attached to one side of the substrate. Therefore, Venkat et al. is not concerned with the precise alignment of the sensor and substrate.

In Bauer et al., since the conductive strip used to attach to the bump bonds is relatively wide, Bauer is silent regarding the issue of alignment. Moreover, in many of the illustrated embodiments, conventional wire contacts **32** are used for aligning the optical sensor **22** with the substrate **28**.

In Casson et al., self-alignment of the solder bump with the flip chip is based on the solder paste mixing with the solder bumps during the heating. This requires an unobstructed motion of the flip chip during reflow - and inclusion of an opening in the mounting substrate adjacent the flip chip would impede the reflow of the solder paste.

It thus appears that the Examiner is using impermissible hindsight reconstruction to modify the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent. The prior art references, individually or in combination, do not teach or suggest a mounting substrate also having an opening therethrough and at least one landing adjacent the opening, and attaching the sensor to the mounting substrate via at least one bump bond interposed between the at least one signal output contact of the sensor and the at least one signal input contact of the mounting substrate to pass signals therethrough, with the at least one bump bond being associated with the at least one landing so that the at least one bump bond is aligned with the at least one signal

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

output contact of the sensor.

Independent Claim 39 recites that the at least one bump bond is associated with the at least one landing so that the at least one bump bond is aligned with the at least one signal output contact of the sensor. The at least one landing and bump bond are provided as spots at specific locations. This specific arrangement of spot lands and bump bonds may provide an advantageous effect of improving the alignment of the image sensor with the mounting substrate. The bump bonds may be heated to melt the solder to make an electrical connection between the signal output contacts of the image sensor **14** and the PCB lands **18**, as shown in FIG. 1 associated with the Applicants' specification. As the spot bump bonds melt they try to minimize forces in their surface tension and thus deform evenly. There is thus a net effect of this action to draw the image sensor into a precise alignment with the aperture.

The bump bonds and landings adjacent the opening in the mounting substrate in the claimed invention thus provide an advantageous effect of actually improving the alignment of the sensor with the mounting substrate. This is not intuitively the case, as movement caused by the melting of the bump bonds would have normally been considered by one skilled in the art at the time of the invention to introduce a further inaccuracy or source of error in the alignment. However, the Applicants have found that counter to these expectations, the bump bonds actually help with the alignment.

Accordingly, it is submitted that independent Claim 39

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

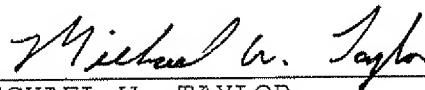
is patentable over the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent. Independent Claim 57 is similar to independent Claim 39. Therefore, it is submitted that this claim is also patentable over the Venkat et al. patent in view of the Bauer et al. patent and in further view of the Casson et al. patent.

In view of the patentability of independent Claims 39 and 57, it is submitted that the dependent claims, which include yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

IV. CONCLUSION

In view of the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



MICHAEL W. TAYLOR

Reg. No. 43,182

Allen, Dyer, Doppelt, Milbrath
& Gilchrist, P.A.

255 S. Orange Avenue, Suite 1401

In re Patent Application of:

RAYNOR ET AL.

Serial No. **10/677,850**

Confirmation No. **5132**

Filed: **October 2, 2003**

Post Office Box 3791
Orlando, Florida 32802
407-841-2330